CLAIMS

While the invention has been described with reference to particular example embodiments, further modifications and improvements which will occur to those skilled in the art, may be made within the purview of the appended claims, without departing from the scope of the invention in its broader aspect.
Numerous modification and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

What is claimed is:

1. A digital phase detector, wherein the digital phase detector comprises:
a frame measurement configuration for counting the first signal clock during every frame of a second signal, and for buffering the counted value until it is read by a phase processing unit.

2. A digital phase detector as claimed in claim 1, wherein:
a nominal number of first signal clocks which corresponds to a zero phase skew between the first signal and the second signal, is subtracted from the counted number of the first signal clocks, in order to calculate an approximate frame skew.

3. A digital phase detector as claimed in claim 1, wherein:
a number of first signal clocks which equals to zero minus the nominal number of first signal clocks, is preset in a counter of the first signal clock before the first clock counting for every second signal frame.

4. A digital phase detector as claimed in claim 1, further comprising:
a phase capture register for capturing a state of outputs of serially connected gates which the first signal clock is propagated through, at the leading edge of the second signal frame.

5. A digital phase detector as claimed in claim 1, further comprising:
a phase capture register for capturing a rise of the second signal frame by multiple outputs of serially connected gates which the first signal clock is propagated through.

6. A digital phase detector as claimed in claim 1, further comprising:
a phase capture register for capturing a state of outputs of serially connected gates which the second signal frame is propagated through, by the leading edge of the first signal clock.

7. A digital phase detector as claimed in claim 1, further comprising:
a phase capture register for capturing a rise of the first signal clock, by multiple outputs of serially connected gates which the second signal frame is propagated through.

8. A digital phase detector as claimed in claim 4 or in claim 5 or in claim 6 or in claim 7, wherein the digital phase detector comprises:
an open ended line of serially connected components which are used as the serially connected gates.

9. A digital phase detector as claimed in claim 4 or in claim 5 or in claim 6 or in claim 7, wherein the digital phase detector comprises:
a ring oscillator which gates are used as the serially connected gates.

10. A digital phase detector as claimed in claim 4 or in claim 5 or in claim 6 or in claim 7, wherein the digital phase detector comprises:
a delay locked loop which gates are used as the serially connected gates.

11. A digital phase detector as claimed in claim 1, the digital phase detector comprising:
a first phase counter buffer for counting first signal clocks during every odd cycle of the second signal frame, and for buffering the counted clocks number during every following even cycle of the second signal frame;
a second phase counter buffer for counting first signal clocks during every even cycle of the second signal frame, and for buffering the counted clocks number during every following odd cycle of the second frame.

12. A digital phase detector as claimed in claim 11, wherein the digital phase detector comprises:
a detector timing circuit for controlling the counting and the buffering functions of the first and the second phase counter buffers.

13. A digital phase detector as claimed in claim 11, wherein said detector timing circuit further comprises:
detection of a beginning of a cycle of the second signal frame;
switching the counter buffers into the counting and buffering operations;
requesting the phase processing unit to read the buffered count numbers;

14. A digital phase detector as claimed in claim 11, wherein:
the first counter buffer is reset after its content is read by a phase processing unit;
the second counter buffer is reset after its content is read by the phase processing unit.

15. A digital phase detector as claimed in claim 14, wherein:
the nominal number of first signal clocks which corresponds to a zero phase skew between the first signal and the second signal, is subtracted by the phase processing unit from the read content of any counter buffer.

16. A digital phase detector as claimed in claim 11, wherein:
the first counter buffer is preset to zero minus the nominal number of first signal clocks,

after its content is read by the phase processing unit;
the second counter buffer is preset to zero minus the nominal number of first signal clocks, after its content is read by the phase processing unit.

17. A digital phase detector as claimed in claim 1, wherein:
said first clock counting is enabled by opening a logical gate which controls an application of the first clock to counter's clocking input;
said first clock counting is disabled by closing a logical gate which controls an application of the first clock to counter's clocking input.

18. A digital phase detector as claimed in claim 4 or in claim 5 or in claim 6 or in claim 7, wherein:
a content of the phase capture register is used to calculate a phase skew difference between the last rise of the first signal clock and the beginning of a new second signal frame;
a content of the phase capture register is used to calculate a remaining phase skew between the beginning of a new second signal frame and the first rise of the first signal clock.

19. A digital phase detector as claimed in claim 18, wherein:
the phase skew difference is added to the present measurement of a phase skew between the first signal and the second signal, wherein the present measurement applies to the present frame period of the second signal;
the remaining phase skew is added to the next measurement of a phase skew between the first signal and the second signal, wherein the next measurement applies to the next frame period of the second signal.

20. A digital phase detector as claimed in claim 18, wherein:
the remaining phase skew is calculated as equal to the first signal clock period minus the phase skew difference.

21. A digital phase detector as claimed in claim 18, wherein:
a content of the phase capture register is used to upgrade the counted number of first signal clocks to an actual number of first signal clocks which really occurred during the second signal frame.

22. A digital phase detector as claimed in claim 8, wherein the digital phase detector comprises a calibration method of gates propagation delays, wherein:
a number of the serially connected gates which represents a number of half cycle times of the first signal clock, is captured in the phase capture register;
the number of half cycle times of the first signal clock, is divided by the captured number.

23. A digital phase detector as claimed in claim 22, wherein the calibration method comprises:

a statistical averaging of a result of the calibration, in order to eliminate most of a granularity error caused by capturing of an integer and to reduce an error caused by a power supply ripple.

24. A digital phase detector as claimed in claim 23, wherein the calibration method further comprises:
assigning higher weights for the captured number of gates, if the captured number is provided by serially connected gates which are located at the front of the delay line;
using the weighted cycle gate numbers for the statistical averaging of the calibration result.

25. A digital phase detector as claimed in claim 4 or in claim 5 or in claim 6 or in claim 7, wherein the digital phase detector comprises:
a first phase counter buffer for counting first signal clocks during every odd cycle of the second signal frame, and for buffering the counted clocks number during every following even cycle of the second signal frame;
a second phase counter buffer for counting first signal clocks during every even cycle of the second signal frame, and for buffering the counted clocks number during every following odd cycle of the second frame.
a detector timing circuit for switching the counting and the buffering functions of the first and the second phase counter buffer.

26. A digital phase detector as claimed in claim 25, wherein:
the switching performed by the detector timing circuits is driven by the first signal clock and is conditioned by a content of the phase capture register.

27. A digital phase detector as claimed in claim 25, wherein:
the phase capture register and some of the flip-flops of the detector timing control, are reset outside of a close time range which surrounds a rising edge of every second signal frame.

28. A digital phase detector as claimed in claim 25, wherein:
if a rising edge of the second signal frame encounters a high level of the first signal clock, the second falling edge of the first signal clock will reverse the counting and the buffering functions of the first and the second phase counter buffer;
if a rising edge of the second signal frame encounters a low level of the first signal clock, the first falling edge of the first signal clock will reverse the counting and the buffering functions of the first and the second phase counter buffer.

29. A digital phase detector as claimed in claim 25, wherein the detector timing circuit comprises a function switching flip-flop, wherein:
the function switching flip-flop switched to 1, inhibits counting in the first counter buffer and enables counting in the second counter buffer;
the function switching flip-flop switched to 0, inhibits counting in the second counter buffer and enables counting in the first counter buffer.

30. A digital phase detector as claimed in claim 11, wherein the digital phase detector further comprises:
a detector timing circuit for switching the counting and the buffering functions of the first and the second phase counter buffer.

31. A digital phase detector as claimed in claim 30, wherein the detector timing circuit further comprises a function switching flip-flop, wherein:
the function switching flip-flop switched to 1, inhibits counting in the first counter buffer and enables counting in the second counter buffer;
the function switching flip-flop switched to 0, inhibits counting in the second counter buffer and enables counting in the first counter buffer.

32. A digital phase detector as claimed in claim 31, wherein the digital phase detector further comprises:
a phase capture register for capturing a state of outputs of serially connected gates which the first signal clock is propagated through, at the leading edge of the second signal frame;
an open ended line of serially connected components which are used as the serially connected gates.

33. A digital phase detector as claimed in claim 31, wherein the digital phase detector further comprises:
a phase capture register for capturing a state of outputs of serially connected gates which the first signal clock is propagated through, at the leading edge of the second signal frame;
a ring oscillator which gates are used as the serially connected gates.

34. A digital phase detector as claimed in claim 31, wherein the digital phase detector further comprises:
a phase capture register for capturing a rise of the first signal clock, by multiple outputs of serially connected gates which the second signal frame is propagated through;
an open ended line of serially connected components which are used as the serially connected gates.

35. A digital phase detector as claimed in claim 31, wherein the digital phase detector further comprises:
a phase capture register for capturing a state of outputs of serially connected gates which the second signal frame is propagated through, by the leading edge of the first signal clock.
an open ended line of serially connected components which are used as the serially connected gates.

36. A digital phase detector as claimed in claim 31, wherein the digital phase detector further comprises:

a phase capture register for capturing a rise of the second signal frame by multiple outputs of serially connected gates which the first signal clock is propagated through;
an open ended line of serially connected components which are used as the serially connected gates.

37. A digital phase detector as claimed in claim 31, wherein the digital phase detector further comprises:
a phase capture register for capturing a rise of the second signal frame by multiple outputs of serially connected gates which the first signal clock is propagated through;
a ring oscillator which gates are used as the serially connected gates.

38. A digital phase detector as claimed in claim 32 or in claim 33 or in claim 34 or in claim 35 or in claim 36 or in claim 37, wherein:
an approximate frame skew is calculated as equal to the counted number of clock cycles minus the nominal number of first signal clocks;
a content of the phase capture register is used to calculate a phase skew difference between the last rise of the first signal clock and the beginning of a new second signal frame;
a content of the phase capture register is used to calculate a remaining phase skew between the beginning of a new second signal frame and the first rise of the first signal clock;
a high resolution extension is calculated by adding the remaining phase skew of the previous measurement to the phase skew difference of the present measurement;
a high resolution frame skew is calculated by adding the approximate frame skew to the high resolution extension.

39. A digital phase detector as claimed in claim 32 or in claim33, wherein:
bit 0 of the phase capture register is set to 1, if a rising edge of the second signal frame encounters a high level of the first signal clock;
bit 1 of the phase capture register is set to 1, if a rising edge of the second signal frame encounters a low level of the first signal clock;
if the bit 0 is set to 1, it enables a second falling edge of the first signal clock to reverse the function switching flip-flop;
if the bit 1 is set to 1, it enables a first falling edge of the first signal clock to reverse the function switching flip-flop.

40. A digital phase detector as claimed in claim 34, wherein:
bit 0 of the phase capture register is set to 1, if a rising edge of the second signal frame encounters a high level of the first signal clock;
bit -1 of the phase capture register is set to 1, if a rising edge of the second signal frame encounters a low level of the first signal clock;
if the bit 0 is set to 1, it enables a second falling edge of the first signal clock to reverse the function switching flip-flop;
if the bit -1 is set to 1, it enables a first falling edge of the first signal clock to reverse the function switching flip-flop.

41. A digital phase detector as claimed in claim 35 or in claim36 or in claim 37, wherein:
bit -1 of the phase capture register is set to 1, if a falling edge of the first signal clock encounters a high level of the second signal frame before a rising edge of the first signal clock does;
bit 0 of the phase capture register is set to 1, if a rising edge of the first signal clock encounters a high level of the second signal frame before a falling edge of the first signal clock does;
if the bit -1 is set to 1, it enables a second falling edge of the first signal clock to reverse the function switching flip-flop;
if the bit 0 is set to 1, it enables a first falling edge of the first signal clock to reverse the function switching flip-flop.